Reg. No. : | | | | | | | | | | | | |

Question Paper Code : X 60441

B.E./B.Tech. DEGREE EXAMINATIONS, NOVEMBER/DECEMBER 2020
Third Semester
Electronics and Communication Engineering
EC 2203/EC 34/080290010/10144 EC 304 – DIGITAL ELECTRONICS
(Regulations 2008/2010)
(Common to PTEC 2203 – Digital Electronics for B.E. (Part-Time)
Third Semester – Electronics and Communication Engineering –
Regulations 2009)

Time : Three Hours | Maximum : 100 Marks

Answer ALL questions

PART – A **(10×2=20 Marks)**

1. Simplify the given Boolean expression using De Morgan's theorem $F = \overline{A\left(\overline{B + \bar{C}}\right)D}$.

2. Design a 3 input CMOS NAND gate.

3. Give the logic expressions for sum and carry in full adder circuit.

4. Give examples for combinational circuit (any four).

5. State the status of the JK flip flop if suppose the setup and holding time is not met.

6. List the advantage and disadvantages of ripple counters.

7. What is the disadvantage of dynamic RAM cell ?

8. How PAL differs from ROM ?

9. What is Synchronous Sequential Circuit ?

10. Write short notes on Hazards.

PART – B **(5×16=80 Marks)**

11. a) i) Reduce the following expression in SOP and POS forms using Karnaugh map. $f = \Sigma m(0, 2, 3, 10, 11, 12, 13, 16, 17, 18, 19, 20, 21, 26, 27)$. **(10)**

ii) Simplify the following function and implement them with two-level NAND gate circuits. **(6)**
F(A, B, C, D) = A′B′C + AC + ACD + ACD′ + A′B′D′ + B′CD.

(OR)

b) i) Obtain the minimal expression using the tabular method and implement it in universal logic. **(10)**
Π M (6, 7, 8, 9). d(10, 11, 12, 13, 14, 15).

ii) Prove that two open – collector TTL inverters, when connected together produce the NOR function. **(6)**

12. a) Design a combinational circuit that converts 4 bit Gray Code to a 4 bit binary number. Implement the circuit. **(16)**

(OR)

b) Detail the following :
i) BCD adder. **(8)**
ii) Magnitude comparator. **(8)**

13. a) i) Design a 4 bit asynchronous up/down counter using JK flipflops. **(8)**

ii) Design a mod-10 synchronous counter using D-flipflips. **(8)**

(OR)

b) i) Draw the logic diagram of a 4-bit universal shift register and explain its operation. **(10)**

ii) Design a 4 bit serial adder. **(6)**

14. a) Discuss in detail about the classifications of memories. **(16)**

(OR)

b) Discuss in detail about the FPGA with suitable diagrams. **(16)**

15. a) i) Write the verilog HDL code for ‘JK’FF and ‘T’FF. **(6)**

ii) An asynchronous circuit with output changing on each rising edge of its input clock. Draw the hazard free circuit. **(10)**

(OR)

b) i) Draw the general model of a sequential circuit and explain. **(6)**

ii) List out the steps involved in the design of synchronous sequential circuit. **(10)**

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